WE CLAIM:

1. A circuit for correcting an asymmetric signal, said circuit comprising:

   a variable gain amplifier circuit for receiving said asymmetric signal and providing first and second outputs; and

   a g_m switch coupled to the first output of the variable gain amplifier circuit and providing an output having only a first polarity,

   wherein the second output of the variable gain amplifier circuit and the output of the g_m switch are combined to provide a corrected signal.

2. The circuit of claim 1, wherein said g_m switch comprises:

   a first switching circuit;

   a second switching circuit; and

   a differential amplifier coupled to said first and second switching circuits.

3. The circuit of claim 2, wherein each of said first and second switching circuits comprises at least one transistor operated in saturation.

4. The circuit of claim 1, wherein said variable gain amplifier circuit comprises first and second variable gain amplifiers coupled in series and providing said first and second outputs, respectively.

5. The circuit of claim 1, wherein said variable gain amplifier circuit comprises a two-stage variable gain amplifier, a first stage providing said first output and a second stage providing said second output.

6. The circuit of claim 1, wherein the g_m switch comprises:

   a transconductance circuit for receiving the asymmetric signal and for providing a current proportional to the asymmetric signal in a first and a second current path;

   a first switching circuit, having a first and a second input, said first switching circuit being coupled to the first current path;

   a second switching circuit, having a third and a fourth input, said second switching circuit being coupled to the second current path;

   a first current source coupled to the first and the third inputs;

   a second current source coupled to the second and fourth inputs; and

   a third current source coupled to the transconductance circuit,

wherein the first switching circuit is responsive to the asymmetric signal for switching the first current source to the first current path or to the second current path, and

wherein the second switching circuit is responsive to the asymmetric signal for switching the second current source to the first current path or to the second current path.

7. The circuit of claim 6, wherein the first switching circuit is responsive to a polarity of the asymmetric signal.

8. The circuit of claim 7, wherein the first switching circuit switches the first input to the first current path when the polarity is positive.

9. The circuit of claim 7, wherein the first switching circuit switches the second input to the first current path when the polarity is negative.

10. The circuit of claim 6, wherein the second switching circuit is responsive to a polarity of the asymmetric signal.

11. The circuit of claim 10, wherein the second switching circuit switches the third input to the second current path when the polarity is negative.

12. The circuit of claim 10, wherein the second switching circuit switches the fourth input to the second current path when the polarity is positive.

13. The circuit of claim 6, wherein the first switching circuit further comprises a pair of field effect transistors arranged to have a sufficiently small linear range to enable the transistors to operate as a switch.

14. The circuit of claim 6, wherein the second switching circuit further comprises a pair of field effect transistors arranged to have a sufficiently small linear range to enable the transistors to operate as a switch.

15. A read channel comprising a circuit for correcting an asymmetric signal from said MR head, said circuit comprising:

a variable gain amplifier circuit for receiving said asymmetric signal from said MR head and providing first and second outputs; and

a g_m switch coupled to the first output of the first variable gain amplifier circuit and providing an output having only a first polarity,

wherein the second output of the variable gain amplifier circuit and the output of the g_m switch are combined to provide a corrected signal.

16. The read channel of claim 15, wherein said g_m switch comprises:

a first switching circuit;

a second switching circuit; and

a differential amplifier coupled to said first and second switching circuits.

17. The read channel of claim 16, wherein each of said first and second switching circuits comprises at least one transistor operated in saturation.

18. The read channel of claim 15, wherein said variable gain amplifier circuit comprises first and second variable gain amplifiers coupled in series and providing said first and second outputs, respectively.

19. The read channel of claim 15, wherein said variable gain amplifier circuit comprises a two-stage variable gain amplifier, a first stage providing said first output and a second stage providing said second output.

20. The read channel of claim 15, wherein the g_m switch comprises:

a transconductance circuit for receiving the asymmetric signal and for providing a current proportional to the asymmetric signal in a first and a second current path;

a first switching circuit, having a first and a second input, said first switching circuit being coupled to the first current path;

a second switching circuit, having a third and a fourth input, said second switching circuit being coupled to the second current path;

a first current source coupled to the first and the third inputs;

a second current source coupled to the second and fourth inputs; and

a third current source coupled to the transconductance circuit,

wherein the first switching circuit is responsive to the asymmetric signal for switching the first current source to the first current path or to the second current path, and

wherein the second switching circuit is responsive to the asymmetric signal for switching the second current source to the first current path or to the second current path.

21. The read channel of claim 20, wherein the first switching circuit is responsive to a polarity of the asymmetric signal.

22. The read channel of claim 21, wherein the first switching circuit switches the first input to the first current path when the polarity is positive.

23. The read channel of claim 21, wherein the first switching circuit switches the second input to the first current path when the polarity is negative.

24. The read channel of claim 20, wherein the second switching circuit is responsive to a polarity of the asymmetric signal.

25. The read channel of claim 24, wherein the second switching circuit switches the third input to the second current path when the polarity is negative.

26. The read channel of claim 24, wherein the second switching circuit switches the fourth input to the second current path when the polarity is positive.

27. The read channel of claim 20, wherein the first switching circuit further comprises a pair of field effect transistors arranged to have a sufficiently small linear range to enable the transistors to operate as a switch.

28. The read channel of claim 20, wherein the second switching circuit further comprises a pair of field effect transistors arranged to have a sufficiently small linear range to enable the transistors to operate as a switch.

29. A hard disk drive comprising:

at least one disk having a surface for storing data thereon;

at least one magneto-resistive (MR) read head for reading information recorded in data tracks on the at least one disk;

a servo actuator for positioning the at least one MR head with respect to the at least one disk; and

a read channel for transmitting data from the at least one MR head;

wherein the read channel comprises a circuit for correcting an asymmetric signal received from said MR head, said circuit comprising:

a variable gain amplifier circuit for receiving said asymmetric signal and providing first and second outputs; and

a g_m switch coupled to the first output of the first variable gain amplifier circuit and providing an output having only a first polarity,

wherein the second output of the variable gain amplifier circuit and the output of the g_m switch are combined to provide a corrected signal.

30. The hard disk drive of claim 29, wherein said g_m switch comprises:

a first switching circuit;

a second switching circuit; and

a differential amplifier coupled to said first and second switching circuits.

31. The hard disk drive of claim 30, wherein each of said first and second switching circuits comprises at least one transistor operated in saturation.

32. The hard disk drive of claim 29, wherein said variable gain amplifier circuit comprises first and second variable gain amplifiers coupled in series and providing said first and second outputs, respectively.

33. The hard disk drive of claim 29, wherein said variable gain amplifier circuit comprises a two-stage variable gain amplifier, a first stage providing said first output and a second stage providing said second output.

34. The hard disk drive of claim 29, wherein the g_m switch comprises:

a transconductance circuit for receiving the asymmetric signal and for providing a current proportional to the asymmetric signal in a first and a second current path;

a first switching circuit, having a first and a second input, said first switching circuit being coupled to the first current path;

a second switching circuit, having a third and a fourth input, said second switching circuit being coupled to the second current path;

a first current source coupled to the first and the third inputs;

a second current source coupled to the second and fourth inputs; and

a third current source coupled to the transconductance circuit,

wherein the first switching circuit is responsive to the asymmetric signal for switching the first current source to the first current path or to the second current path, and

wherein the second switching circuit is responsive to the asymmetric signal for switching the second current source to the first current path or to the second current path.

35. The hard disk drive of claim 34, wherein the first switching circuit is responsive to a polarity of the asymmetric signal.

36. The hard disk drive of claim 35, wherein the first switching circuit switches the first input to the first current path when the polarity is positive.

37. The hard disk drive of claim 35, wherein the first switching circuit switches the second input to the first current path when the polarity is negative.

38. The hard disk drive of claim 34, wherein the second switching circuit is responsive to a polarity of the asymmetric signal.

39. The hard disk drive of claim 38, wherein the second switching circuit switches the third input to the second current path when the polarity is negative.

40. The hard disk drive of claim 38, wherein the second switching circuit switches the fourth input to the second current path when the polarity is positive.

41. The hard disk drive of claim 34, wherein the first switching circuit further comprises a pair of field effect transistors arranged to have a sufficiently small linear range to enable the transistors to operate as a switch.

42. The hard disk drive of claim 34, wherein the second switching circuit further comprises a pair of field effect transistors arranged to have a sufficiently small linear range to enable the transistors to operate as a switch.

43. A method of correcting an asymmetric signal, said method comprising:
sending said asymmetric signal through a variable gain amplifier circuit;
sending a first output of said variable gain amplifier circuit through a g_m switch coupled to the first output of the variable gain amplifier circuit, wherein an output of said g_m switch has only a first polarity; and
combining a second output of the variable gain amplifier circuit and the output of the g_m switch to provide a corrected signal.

44. The method of claim 43, wherein sending the first output of said variable gain amplifier circuit through the g_m switch comprises:

sending the asymmetric signal through a transconductance circuit and providing a current proportional to the asymmetric signal in a first and a second current path; and

responsive to a polarity of the asymmetric signal, switching first and second current sources to said first current path or said second current path.

45. A circuit for correcting an asymmetric signal, said circuit comprising:

means for receiving said asymmetric signal and providing first and second variable gain outputs; and

switching means coupled to the first variable gain output and providing an output having only a first polarity,

wherein the second variable gain output and the output of the switch means are combined to provide a corrected signal.

46. The circuit of claim 45, wherein said switching means comprises:

a first switching circuit;

a second switching circuit; and

a differential amplifier coupled to said first and second switching circuits.

47. The circuit of claim 46, wherein each of said first and second switching circuits comprises at least one transistor operated in saturation.

48. The circuit of claim 45, wherein said means for receiving said asymmetric signal comprises first and second variable gain amplifiers coupled in series and providing said first and second variable gain outputs, respectively.

49. The circuit of claim 45, wherein said means for receiving said asymmetric signal comprises a two-stage variable gain amplifier, a first stage providing said first variable gain output and a second stage providing said second variable gain output.

50. A read channel comprising a circuit for correcting an asymmetric signal from said MR head, said circuit comprising:

means for receiving said asymmetric signal and providing first and second variable gain outputs; and

switching means coupled to the first variable gain output and providing an output having only a first polarity,

wherein the second variable gain output and the output of the switch means are combined to provide a corrected signal.

51. The read channel of claim 50, wherein said switching comprises:

a first switching circuit;

a second switching circuit; and

a differential amplifier coupled to said first and second switching circuits.

52. The read channel of claim 51, wherein each of said first and second switching circuits comprises at least one transistor operated in saturation.

53. The read channel of claim 50, wherein said means for receiving said asymmetric signal comprises first and second variable gain amplifiers coupled in series and providing said first and second variable gain outputs, respectively.

54. The read channel of claim 50, wherein said means for receiving said asymmetric signal comprises a two-stage variable gain amplifier, a first stage providing said first variable gain output and a second stage providing said second variable gain output.

55. A hard disk drive comprising:

means for storing data;

reading means for reading information from the means for storing data;

means for positioning the reading means with respect to the means for storing data; and

means for transmitting data from the reading means;

wherein the means for transmitting data comprises means for correcting an asymmetric signal received from the reading means, said means for correcting comprising:

means for receiving said asymmetric signal and providing first and second variable gain outputs; and

switching means coupled to the first variable gain output and providing an output having only a first polarity,

wherein the second variable gain output and the output of the switch means are combined to provide a corrected signal.

56. The hard disk drive of claim 55, wherein said switching means comprises:
a first switching circuit;
a second switching circuit; and
a differential amplifier coupled to said first and second switching circuits.

57. The hard disk drive of claim 56, wherein each of said first and second switching circuits comprises at least one transistor operated in saturation.

58. The hard disk drive of claim 55, wherein said means for receiving said asymmetric signal comprises first and second variable gain amplifiers coupled in series and providing said first and second variable gain outputs, respectively.

59. The hard disk drive of claim 55, wherein said means for receiving said asymmetric signal comprises a two-stage variable gain amplifier, a first stage providing said first variable gain output and a second stage providing said second variable gain output.